Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations August-2021

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Convert the following numbers i) $(41.6875)_{10}$ to Hexadecimal number ii) $(11001101.0101)_2$ to base-8 and base-4 iii) $(4567)_{10}$ to base2	**6M**
	b	Subtract $(111001)_2$ from (101011) using 1's complement?	**6M**
		OR	
2	**a**	The solution to the quadratic equation x^2-11x+22=0 is x=3 and x=6 what is the base of the number	**6M**
	b	Write about Error correction & Detection?	**6M**
		UNIT-II	
3		Simplify the following Boolean expression using K-MAP and implement using NAND gates. F(W,X,Y,Z) = XYZ+WXY+WYZ+WXZ	**12M**
		OR	
4		Obtain the minimal product of sums and design using NAND gates F(A,B,C,D)= = $\sum$m(0,2,3,6,7) +d(8,10,11,15)	**12M**
		UNIT-III	
5	**a**	Explain about Binary Half Adder?	**5M**
	b	What is Full Adder? Design & Explain the operations of Full Adder ?	**7M**
		OR	
6	**a**	Design a 4 bit adder-subtractor circuit and explain the operation in detail?	**7M**
	b	Explain the functionality of a Multiplexer?	**5M**
		UNIT-IV	
7	**a**	Explain the Logic diagram of SR flip-flop?	**6M**
	b	Design and draw the 3 bit up-down synchronous counter?	**6M**
		OR	
8		Explain the design of a 4 bit binary counter with parallel load in detail?	**12M**
		UNIT-V	
9		Design PAL for a combinational circuit that squares a 3 bit number?	**12M**
		OR	
10		Construct the PROM using the conversion from BCD code to Excess-3 code?	**12M**

*** END ***